**Experiment: 7**

Name: Aaditya Jindal

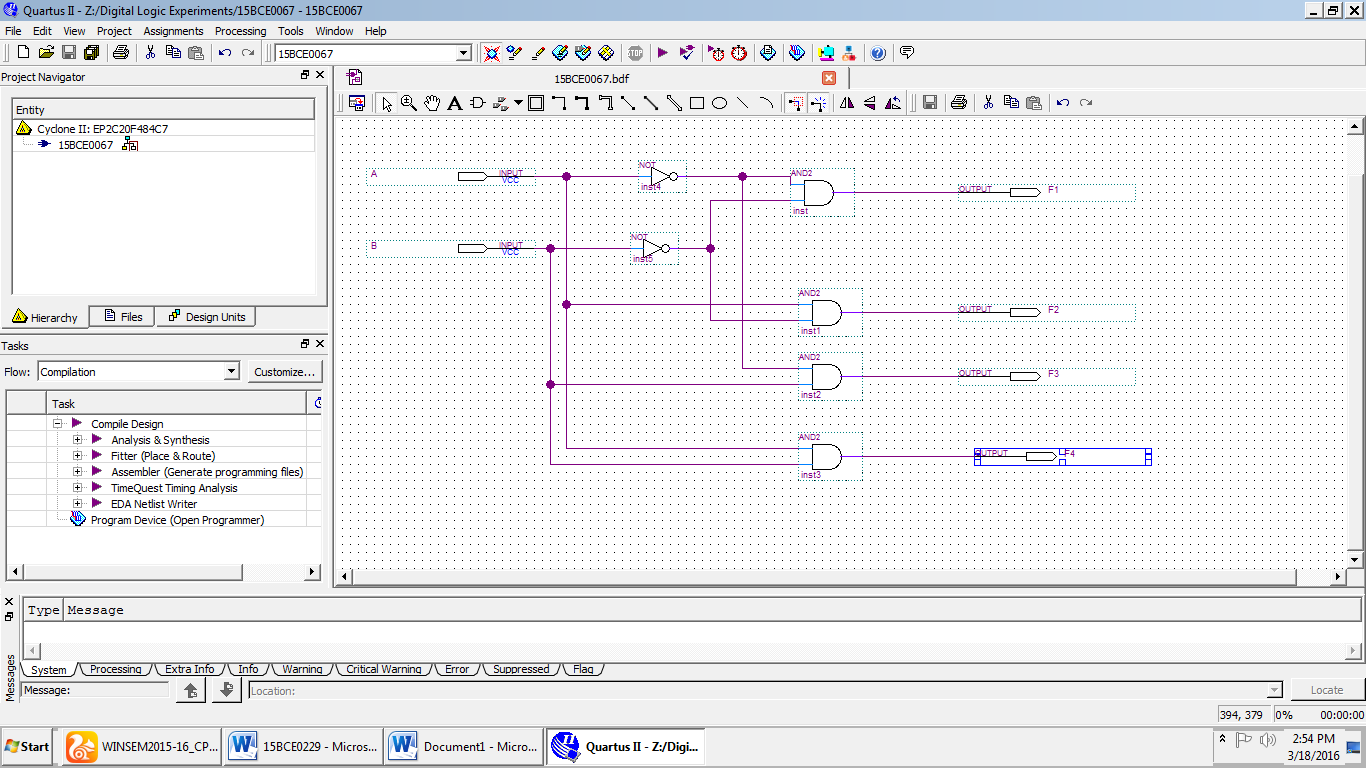
Reg no: 15BCE0067

Slot: L55 + L56

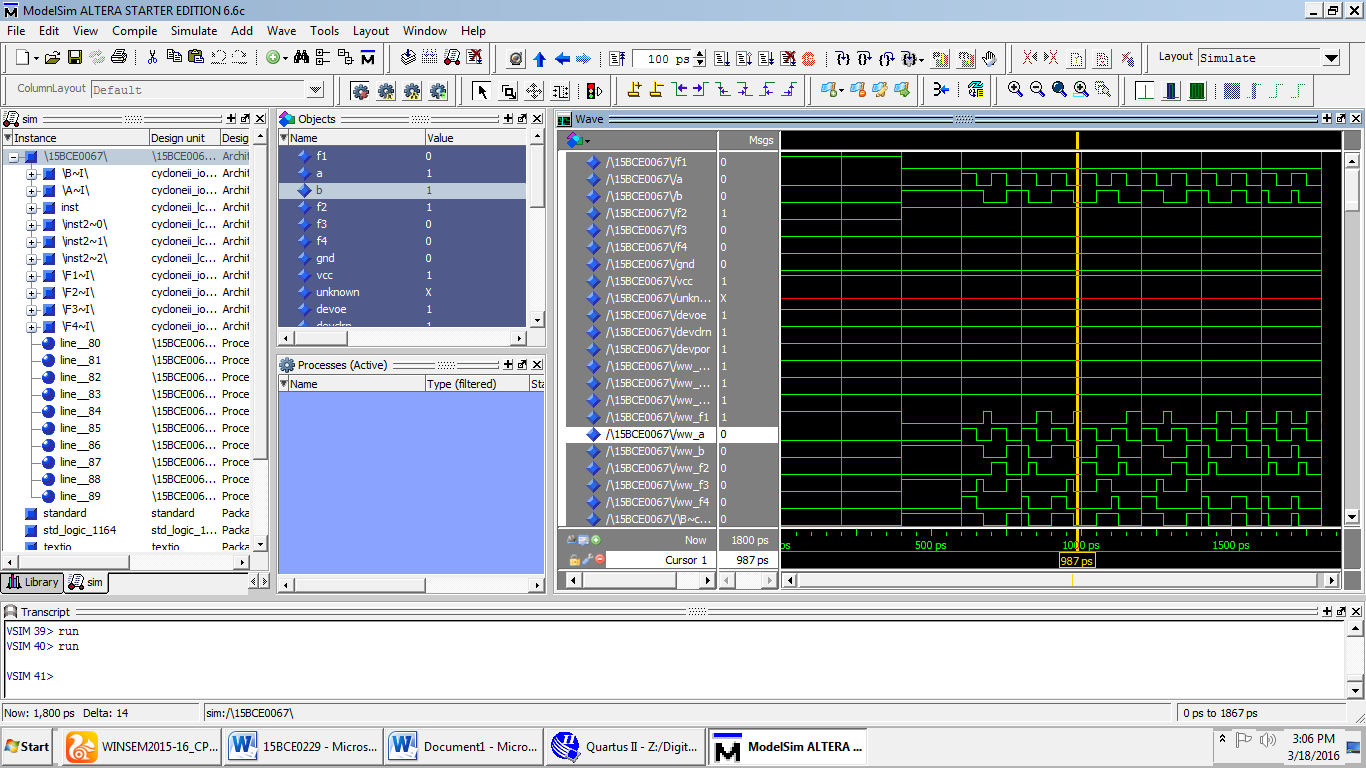
Faculty: I. Mala Serene

**AIM:** To design 2 to 4 line decoder.

**Block Diagram:**



**Wave Output:**



**Truth Table:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | F1 | F2 | F3 | F4 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |